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Docket No.: 0756-2345

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Dividional Application of :	)	
Shunpei YAMAZAKI et al	)	
Application No.: 09/917,633	)	Group Art Unit: 2811
Filed: July 31, 2001	)	Examiner: S. Hu
For : SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	)	

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Noriko Inage, 116-2, Kamiohi, Ohi-machi, Ashigarakami-gun, Kanagawa-ken 258-0016 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 5-48534 filed on February 15, 1993; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 5-48534 filed on February 15, 1993.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that theses statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 20th day of December, 2001

Noriko Inage.

Name: Noriko Inage

[Name of Document] Patent Application
[Reference Number] P002267-04
[Filing Date] February 15, 1993
[Attention] Commissioner, Patent Office
[International Patent Classification] H01L 21/00
[Title of Invention] SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
[Number of Claims] 4
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[Attachment] Specification 1
[Attachment] Drawing 1
[Attachment] Abstract 1

[Name of Document] Specification

[Title of the Invention]

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

[Scope of Claims]

[Claim 1]

A method of fabricating a semiconductor device comprising:

a first step forming a gate insulating film on an island-like semiconductor region and a gate electrode on said gate insulating film;

a second step introducing an impurity into said semiconductor region using said gate electrode as a mask;

a third step adhering a substance containing at least one of nickel, iron, cobalt and platinum on a part of said semiconductor region; and

a forth step annealing said island-like semiconductor region.

[Claim 2]

The method of fabricating a semiconductor device as claimed in claim 1, characterized in that after the forth step, a fifth step of annealing is perofrmed in an atmosphere comprising chlorine at a temperature of 400 to 650℃.

[Claim 3]

The method of fabricating a semiconductor device as claimed in claim 1, characterized in that said substance containing a nickel contains silicon and nickel and its composition ratio of silicon and nickel is 0.4 to 2.5.

[Claim 4]

A thin film transistor comprising a source and/or a drain formed by a silicon semiconductor containing hydrogen at a concentration of more than 0.01 atomic% and less than 5 atomic%, and nickel at the concentration of more than 0.005 atomic% and less than 1 atomic%.

[Detailed Description of the Invention]

[0001]

[Technical field to which the Invention pertains]

The present invention relates to a method of obtaining a crystalline semiconductor used for thin film devices such as a thin film insulated gate type field effect transistor (thin film transistor or TFT).

[0002]

[Prior Art]

Conventionally, a crystalline semiconductor thin film used for thin film devices such as a thin film insulated gate type field effect transistor (TFT) has been fabricated by crystallizing an amorphous silicon film formed by a plasma CVD method or thermal CVD method at a temperature of more than 600℃ in an apparatus such as an electric furnace.

[0003]

[Problem to be Solved by the Invention]

This conventional method, however, has had various problems. The biggest problem has been that it is difficult to obtain a good product because the crystalline silicon film obtained is polycrystal and there is difficultly in controlling its grain boundary, and its reliability and yield is not so high because of its dispersion characteristic. That is, because the silicon crystals obtained by conventional heat treatment grow totally at random, it has been almost impossible to control the direction of its crystal growth.

Accordingly, it is an object of the present invention to solve the aforementioned problems by providing a method for controlling the growth of the crystal.

[0004]

[Means for Solving the Problem]

According to the present invention, crystal growth is controlled, and a TFT having high reliability and high yield is obtained, by forming a gate electrode on a silicon film in an amorphous state or in a random crystal state (for example a state in which portions having good crystallinity and amorphous portions exist in a mixed state) which can be said to be a substantially amorphous state, by forming impurity regions within the silicon film using the gate electrode as a mask, forming regions containing at least one of nickel, iron, cobalt platinum or palladium so that they adhere on part of the impurity regions, and by annealing the whole to crystallize it starting from the region containing nickel.

In particular, the present invention allows substantial elimination of the grain boundary between the source and drain and the active layer and to obtain a good characteristic by advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region).

[0005]

A method of growing a crystal of silicon film epitaxially in solid phase centering on a crystalline island-like film as a nucleus or as a seed crystal has been proposed as a prior art method (for example, Japanese Patent Laid-Open No. 1-214110, etc.). However, it has been difficult to suppress crystal

growth from other sites even if the crystal nucleus exists. That is, because the annealing temperature for growing the crystal is a temperature suited for fully generating the crystal nucleus, the crystal often starts to grow from unexpected locations.

[0006]

The inventor of the present invention found that nickel (Ni), cobalt, iron and platinum are readily coupled with silicon and that the crystal would grow centering on them. The inventor noticed that nickel is readily made into nickel silicide (a chemical formula of NiSix is $0.4 \leqq x \leqq 2.5$) and that the lattice constant of the nickel silicide is close to that of silicon crystal, then devised a method of growing a silicon crystal centering on the nickel silicide. Actually, the crystal growing temperature could be lowered by 20 to 150℃ compared to that of the conventional method. Because no crystal nucleus was produced in a pure silicon film at this temperature, crystals did not grow from unexpected locations. It was assumed that the crystal grew from the crystal nucleus by the same mechanism as the conventional one and that the higher the temperature, the faster the speed of advancement of the crystallization, at temperatures at which crystal nuclei did not grow naturally (preferably less than 580℃). A similar effect was seen also with platinum (Pt), iron (Fe) and cobalt (Co).

[0007]

According to the present invention, a film or the like containing a simple substance of nickel, iron, cobalt, platinum or their silicides is adhered to the impurity regions of the thin film transistor, and the region of the crystal silicon is expanded away therefrom as the starting point. By the way, oxide is not preferable as the material containing the aforementioned material because oxide is a stable compound and a silicide which is likely to become the crystal nucleus is not produced therefrom.

[0008]

The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity. A better result could be obtained with an amorphous silicon film having less hydrogen concentration serving as the starting material for crystallization. However, because hydrogen was released as crystallization advanced, no clear correlation could be seen between the hydrogen concentration within the silicon film obtained and that of the amorphous silicon film as the starting material. The hydrogen concentration within the crystal silicon of the present invention was typically more than 0.01 atomic% and less than 5 atomic%.

[0009]

While a heavy metal material such as nickel, iron, cobalt or platinum is used in the present invention, those material themselves are not suitable for silicon as a semiconductor material. It is

therefore necessary to remove them if those elements are contained in excess. It was found from a result of the study conducted by the inventor that nickel can be fully removed by annealing it in an atmosphere of hydrogen chloride, various methane chlorides (CH_3Cl etc.), various ethane chlorides ($C_2H_3Cl_3$, etc.) and various ethylene chlorides (C_2HCl_3, etc.) at a temperature of 400 to 600℃. It was found that the concentration of nickel, iron, cobalt or platinum within the silicon film of the present invention was preferably set at more than 0.005 atomic% and less than 1 atomic%.

Referring now to the drawings, preferred embodiments of the present invention will be explained.

[0010]

[Embodiment of the Invention]

[Embodiment 1]

A ground silicon oxide film 11 having a thickness of 2000 angstroms was formed on a substrate (Corning 7059) 10 by a plasma CVD method. Further, an amorphous silicon film having a thickness of 200 to 3000 angstroms or preferably 500 to 1500 angstroms was fabricated by a plasma CVD or vacuum CVD method. The amorphous silicon film could be easily crystallized by reducing hydrogen concentration within the film to less than 5 atomic% by dehydrogenizing it by annealing for 0.1 to 2 hours at a temperature of from 350 to 450℃. It was then patterned to form an island-like silicon region 12. Then a silicon oxide film 13 having a thickness of 500 to 1500 angstroms which functions as a gate insulating film was formed by a RF plasma CVD, ECR plasma CVD or sputtering method. A favorable result could be obtained by using TEOS (tetraethoxisillane) and oxygen as original gases when the plasma CVD method was adopted. Then a tantalum film (5000 angstroms thick) containing 1% of silicon was deposited by a sputtering method and was patterned to form gate wiring and an electrode 14. Titanium, silicon, chromium or aluminum may be used as the material of the gate electrode.

[0011]

Then, the substrate was soaked in an ethylene glycol solution of 3% tartaric acid and was anodized by setting platinum as the cathode and tantalum wire as the anode and circulating a current therebetween. The current was applied such that its voltage rises 2V/min. and becomes constant when it reaches 220V. The current was stopped when it was reduced to less than 10 micro A/m^2. As a result, an anodic oxide (tantalum oxide) 15 having a thickness of 2000 angstroms was formed. Similarly, titanium oxide, aluminum oxide or silicon oxide can be obtained as an anodic oxide when titanium, aluminum or silicon is used for the gate electrode (FIG.1(A)).

[0012]

Next, an impurity was introduced by a plasma doping method. For the doping gas, phosphine

(PH_3) was used for an N type TFT and diborane (B_2H_6) was used for a P type TFT. The N type TFT is shown in the figure. The acceleration voltage was 80keV for phosphine and 65keV for diborane. Impurity regions 16A and 16B were thus formed. At this time, the impurity regions and the gate electrode were offset as seen in the figure. Further, holes were created on the silicon oxide film 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B so that they adhere to the semiconductor region 12 through the holes. Then annealing was carried out in a nitrogen atmosphere at a temperature of 550℃ for four hours to crystallize the impurity regions 16 and other semiconductor regions (FIG.1 (B)).

[0013]

Finally, a silicon oxide film having a thickness of 5000 angstroms was deposited as an interlayer insulator 18 in the same manner as the fabrication method of normal TFTs, and contact holes were created therethrough to form wiring and electrodes 19A and 19B on the source and drain regions. Aluminum, titanium, titanium nitride or a multilayer film thereof is suitable for the wiring and electrode material. A multilayer film of titanium nitride (1000 angstroms thick) and aluminum (5000 angstroms thick) was used in this embodiment (FIG.1(C)).

[0014]

The TFT (N-channel type in the figure) was fabricated through the process described above. The field effect mobility of the TFT obtained was 40 to 60cm^2/Vs in the N-channel type and 30 to 50cm^2/Vs in the P-channel type. Further, the threshold voltage, field effect mobility and sub-threshold characteristic barely changed and high reliability could be obtained even when a voltage of from 17 to 25V was applied for 48 hours between the gate and the drain. This is because the source, drain and channel forming region (the semiconductor region under the gate electrode) were crystallized simultaneously and their direction of crystallization is the same.

[0015]

[Embodiment 2]

A ground silicon oxide film 21 having a thickness of 2000 angstroms was formed on a substrate (Corning 7059) 20 by a plasma CVD method. Further, an amorphous silicon film having a thickness of 200 to 3000 angstroms or preferably 500 to 1500 angstroms was fabricated by a plasma CVD or vacuum CVD method. The amorphous silicon film could be easily formed by reducing the hydrogen concentration within the film to less than 5 atomic% by dehydrogenizing it by annealing for 0.1 to 2 hours at a temperature of from 350 to 450℃. It was then patterned to form an island-like silicon region 23. Then a silicon oxide film 24 having a thickness of 500 to 1500 angstroms which functions as a gate

insulating film was formed by a RF plasma CVD, ECR plasma CVD or sputtering method. A favorable result could be obtained by using TEOS (tetraethoxisillane) and oxygen as original gases when the plasma CVD method was adopted. Then a polycrystal silicon film (5000 angstroms thick) containing 1 to 5% of phosphorus was deposited by a LPCVD method and patterned to form gate wiring and electrodes 25A and 25B (FIG.2(A)).

[0016]

After that, an impurity was diffused thereinto by an ion doping method to form N type impurity regions 26A and P type impurity regions 26B. At this time, phosphorus (doping gas is phosphine PH_3) can be used as the N type impurity for example to dope on the whole surface with 60 to 110kV or 80kV of acceleration voltage, for example, and then boron for example (doping gas is diborane B_2H_6) could be used as the P type impurity doped at an acceleration voltage of 40 to 80kV or 65kV, for example, to cover the region of the N channel type TFT by photoresist.

[0017]

Further, holes were created in the silicon oxide film 24 on the impurity regions to form nickel silicide (or nickel) films 27A and 27B having a thickness of 200 to 1000 angstroms or 300 angstroms, for example, so that they adhere to the impurity regions 26 through the holes. Then annealing was carried out in a nitrogen atmosphere at a temperature of 550℃ for four hours to crystallize the impurity regions 26 and other semiconductor regions. At this time, the crystal growth advances from both ends of the island-like semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region and no detrimental effects were imposed on the characteristics of the TFT (FIG.2(B)).

Alternatively, a nickel silicide film 27C may be provided in the middle of the island-like semiconductor region as shown in FIG.2(C). In this case, crystallization advances from the center (FIG.2(C)).

[0018]

Finally, a silicon oxide film having a thickness of 5000 angstroms was deposited as an interlayer insulator 28 in the same manner as the fabrication method of normal TFTs, and contact holes were created therethrough to form wiring and electrodes 29A, 29B and 29C on the source and drain regions. Aluminum, titanium, titanium nitride or a multilayer film thereof is suitable for the wiring and electrode material. A multilayer film of titanium nitride (1000 angstroms thick) and aluminum (5000 angstroms thick) was used in this case (FIG. 2(D)).

The CMOS type TFT was fabricated by the process described above. Then a shift register was

fabricated using a CMOS circuit thus fabricated to study its operating characteristics. As a result, the maximum operating frequency was 11 MHz when the drain voltage was 15V and 18 MHz when the drain voltage was 17V.

[0019]

[Effect of the Invention]

As described above, the present invention allows control of the direction of crystal growth, which has been difficult in the past, and allows remarkable improvement of the reliability and yield of thin film transistors. Further, because the facilities, apparatuses and techniques necessary for the present invention are very general and are excellent in terms of mass-producibility, the present invention contributes an immeasurable benefit to the industry. Thus the present invention is industrially beneficial and worthy of patent.

[Brief Description of the Drawings]

[FIG. 1] Diagrams showing a top view of the present invention. (steps of fabricating TFTs)

[FIG. 2] Cross-sectional views of the present invention. (steps of fabricating TFTs)

[Description of Symbols]

10 a substrate (Corning 7059)

11 a ground oxide film (silicon oxide)

12 an island-like silicon region

13 a gate insulating film (silicon oxide)

14 a gate electrode (tantalum)

15 an anodic oxide (tantalum oxide)

16 an impunity region (n-type)

17 a nikel silicide film

18 an interlayer insulator (silicon oxide)

19 a metal electrode (a multilayer film of titanium nitride and aluminum)

[Document Name] Abstract

[Summary]

[Problem]

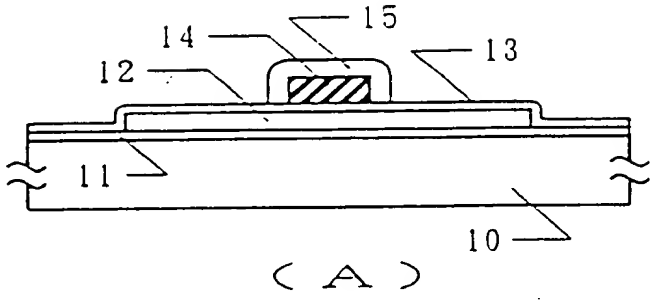
A method for improving the reliability and yield of a thin film transistor by controlling the crystallinity thereof.

[Solving Means]

The method comprises the steps of forming a gate electrode on an island-like amorphous silicon film, injecting an impurity using the gate electrode as a mask, forming a coating film containing at least one of nickel, iron, cobalt and platinum so that it adheres to parts of the impurity regions, and annealing it at a temperature lower than the crystallization temperature of pure amorphous silicon to advance the crystallization starting therefrom and to crystallize the impurity regions and channel forming region.

[Selected Drawing] FIG. 1

[Reference Number] P00 2267-04
[Name of Document] Drawing
[FIG. 1]



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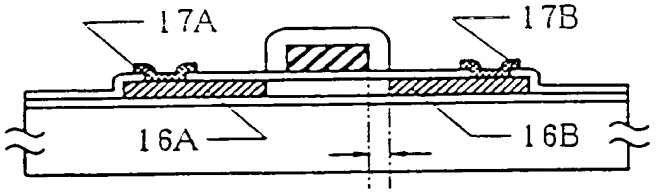

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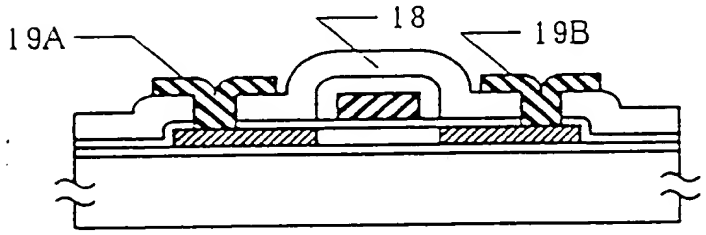

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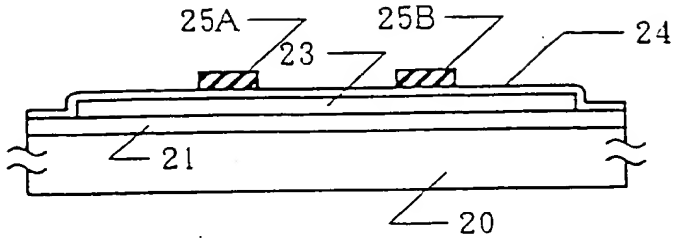
[Reference Number] P002267-04

[FIG. 2]



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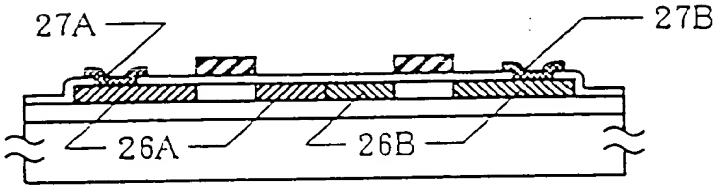

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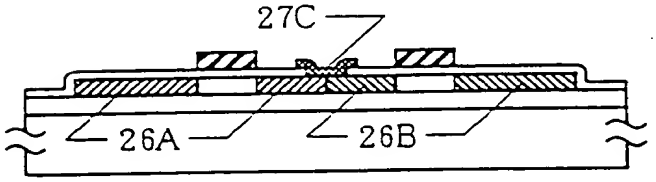

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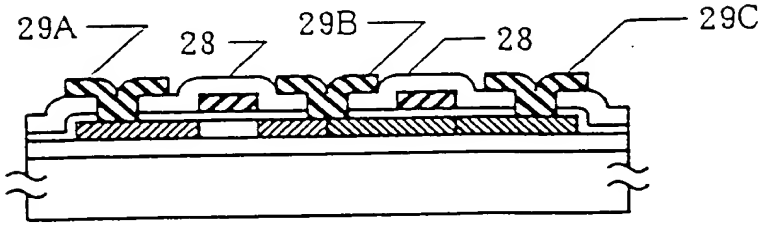

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